Electronic Version
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Claims

[c1] What is claimed is:

1.A method of forming a gate structure comprising:

providing a substrate, and consecutively forming a gate oxide layer, a polysilicon layer, a silicide layer, and a cap layer onto the substrate;

etching a portion of the cap layer, the silicide layer, and the polysilicon layer, and stopping etching on the polysilicon layer to form a stacked gate structure;

removing a portion of the silicide layer exposed on side-walls of the stacked gate structure for forming a recess on the sidewalls of the stacked gate structure;

filling a passivation layer into the recess; and

removing the remaining polysilicon layer and the gate oxide layer outside the sidewalls of the stacked gate structure.

[c2] 2.The method of claim 1 wherein the steps of forming the stacked gate structure further comprises:

coating a photoresist layer onto the cap layer;

performing an exposure process and a development process by a photo mask to remove a portion of the photoresist layer for forming a photoresist pattern; and

utilizing the photoresist pattern as a hard mask to remove the cap layer, the silicide layer, and a portion of the polysilicon layer not covered by the photoresist pattern.

[c3] 3.The method of claim 2 further comprising a step of removing the photoresist pattern after removing the polysilicon layer and the gate oxide layer outside the sidewalls of the stacked gate structure.

[c4] 4.The method of claim 1 wherein forming the stacked gate structure comprises:
forming a patterned silicon oxynitride layer; and
utilizing the patterned silicon oxynitride layer as a hard mask to remove the cap layer, the silicide layer, and a portion of the polysilicon layer not covered by the patterned silicon oxynitride layer.

[c5] 5.The method of claim 4 further comprising a step of removing the patterned polysilicon oxynitride layer after removing the polysilicon layer and the gate oxide layer outside the sidewalls of the stacked gate structure.

[c6] 6.The method of claim 1 wherein the silicide layer comprises tungsten silicon.

[c7] 7.The method of claim 1 wherein the recess is formed by removing a portion of the silicide layer using an ammo-

nium hydrogen peroxide mixture (APM) solution.

[c8] 8.The method of claim 1 wherein the passivation layer comprises silicon nitride.

[c9] 9.The method of claim 1 wherein filling the passivation layer into the recess further comprises:
depositing a silicon nitride layer onto the polysilicon layer and filling the recess; and
performing an anisotropic etching process to remove the silicon nitride layer outside the recess.

[c10] 10.A method of forming a gate structure comprising:
providing a substrate, and consecutively forming a gate oxide layer, a polysilicon layer, a silicide layer, and a cap layer onto the substrate;
forming a patterned mask layer on the cap layer;
etching the cap layer, the silicide layer, and a portion of the polysilicon layer, and stopping etching on the polysilicon layer to form a stacked gate structure;
removing a portion of the silicide layer exposed on sidewalls of the stacked gate structure with an etching solution to form a recess;
depositing a passivation layer onto the polysilicon layer and filling the recess, and performing an anisotropic etching process to remove the passivation layer outside the recess;

removing the polysilicon layer and the gate oxide layer not covered by the patterned mask layer; and
removing the patterned mask layer.

[c11] 11.The method of claim 10 wherein the patterned mask layer comprises silicon oxynitride.

[c12] 12.The method of claim 10 wherein the steps of forming the patterned mask layer comprises:
forming a silicon oxynitride layer on the cap layer;
coating a photoresist layer on the silicon oxynitride;
performing an exposure process and a development process by using a photo mask to form a photoresist pattern;
utilizing the photoresist pattern as a hard mask to remove the silicon oxynitride not covered by the photoresist pattern; and
removing the photoresist pattern.

[c13] 13.The method of claim 10 wherein the silicide layer comprises tungsten silicon.

[c14] 14.The method of claim 10 wherein the etching solution is an ammonium hydrogen peroxide mixture (APM) solution.

[c15] 15.The method of claim 10 wherein the passivation layer comprises silicon nitride.